AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a buffer layer formed on the substrate;

a graded channel layer formed on the buffer layer, said graded channel layer composed of a second compound semiconductor layer doped with an impurity, said second compound semiconductor layer selected from the group consisting of a $In_xGa_{1-x}As$ layer, a $GaAs_{1-x}Sb_x$ layer and a $In_xGa_{1-x}Sb$ layer (x: distribution), the distribution (x) being set to $0.8 \leq x < 1$, ~~of which one constituent element of said second compound semiconductor layer~~ said distribution (x) has a peak ~~distribution~~ in the inside of said graded channel layer in a thickness direction, thereby an energy band gap of the graded channel layer is made narrower in the inside than at both ends in the thickness direction;

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer via the barrier layer.

Claim 2 (Canceled).

Claim 3 (Original): A compound semiconductor device according to claim 1, wherein a peak of the one constituent element in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or positioned at a position that is deviated from the center.

Claim 4 (Original): A compound semiconductor device according to claim 1, wherein a peak of carrier density in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or deviates from the center.

Claim 5 (Previously Presented): A compound semiconductor device according to claim 4, wherein a peak of carrier density in the graded channel layer shifts to the substrate side from a center of layer thickness of the graded channel layer.

Claim 6 (Original): A compound semiconductor device according to claim 1, wherein contact layers are formed between the source electrode and the barrier layer and between the drain electrode and the barrier layer respectively.

Claim 7 (Canceled).

Claim 8 (Currently Amended): A compound semiconductor device according to claim 1, wherein the first compound semiconductor constituting the substrate is GaAs~~, and the second compound semiconductor layer constituting the graded channel layer is an~~

~~InGaAs, and the one constituent element contained in the second compound semiconductor layer is indium~~.

Claims 9 - 11 (Canceled).

Claim 12 (New): A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a buffer layer formed on the substrate;

a graded channel layer formed on the buffer layer, said graded channel layer composed of a second compound semiconductor layer doped with an impurity of which one constituent element of said second compound semiconductor layer has a peak distribution in the inside of said graded channel layer in a thickness direction, thereby an energy band gap of the graded channel layer is made narrower in the inside than at both ends in the thickness direction;

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer via the barrier layer, wherein

the first compound semiconductor constituting the substrate is InP, and the second compound semiconductor layer constituting the graded channel layer is an InAsP or a GaAsSb or an InPSb, and one constituent element contained in the second compound semiconductor layer is indium or antimony.